

STD40N2LH5 STU40N2LH5

N-channel 25 V, 0.01 Ω 40 A, DPAK, IPAK STripFET™ V Power MOSFET

Preliminary Data

Features

Туре	V _{DSS}	R _{DS(on)} max	۱ _D
STD40N2LH5	25 V	0.012 Ω	40 A
STU40N2LH5	25 V	0.0126 Ω	40 A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Application

Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFETTM technology. The lowest available $R_{DS(on)}^*Q_g$, in the standard packages, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

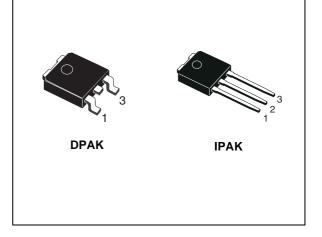


Figure 1. Internal schematic diagram

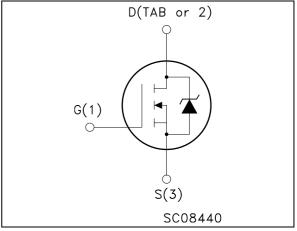


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD40N2LH5	40N2LH5	DPAK	Tape and reel
STU40N2LH5	40N2LH5	IPAK	Tube

1 Electrical ratings

Table 2.	Absolute	maximum	ratings
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Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} =0)	25	V
V _{GS}	Gate-Source voltage	± 22	V
I _D	Drain current (continuous) at $T_C = 25 \ ^{\circ}C$	40	A
I _D	Drain current (continuous) at $T_C = 100 \ ^{\circ}C$	28	A
I _{DM} ⁽¹⁾	Drain current (pulsed)	160	А
P _{TOT}	Total dissipation at $T_{C} = 25 \ ^{\circ}C$	35	W
	Derating factor	0.23	W/°C
E _{AS} ⁽²⁾	Single pulse avalanche energy	TBD	mJ
T _j T _{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width limited by safe operating area

2. Starting Tj = 25 °C, I_D = 24 A, V_{DD} = 12 V

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	4.3	°C/W
Rthj-amb	Thermal resistance junction-case max	100	°C/W
TI	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

Table 4.	Static					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown Voltage	$I_{D} = 250 \ \mu A, \ V_{GS} = 0$	25			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 25 V V _{DS} = 25 V, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ± 22 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 μ A	1			۷
		V _{GS} = 10 V, I _D = 20 A SMD version		0.01	0.012	Ω
Brach	Static drain-source on	V_{GS} = 10 V, I _D = 20 A		0.0106	0.0126	Ω
R _{DS(on)}	resistance	V _{GS} = 5 V, I _D = 20 A SMD version		0.0135	0.017	Ω
		V_{GS} = 5 V, I _D = 20 A		0.0141	0.0176	Ω

Table 4. Static

Symbol	Parameter	Test conditions	Min	Тур.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f=1 MHz, V _{GS} = 0		840 180 29		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} =15 V, I _D = 40 A V_{GS} = 5 V <i>(Figure 3)</i>		8 TBD TBD		nC nC nC
Q _{gs1} Q _{gs2}	Pre V _{th} gate-to-source charge Post V _{th} gate-to-source charge	V _{DD} =15 V, I _D = 40 A V _{GS} = 5 V <i>(Figure 8)</i>		TBD TBD		nC nC
R _G	Gate input resistance	f=1 MHz gate bias Bias= 0 test signal level=20 mV open drain		1.1		Ω



Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on delay time Rise time	V_{DD} = 10 V, I _D = 20 A, R _G = 4.7 Ω , V _{GS} = 10 V (Figure 2 and Figure 7)		TBD TBD		ns ns
t _{d(off)} t _f	Turn-off delay time Fall time	V_{DD} = 10 V, I _D = 20 A, R _G = 4.7 Ω , V _{GS} = 10 V (Figure 2 and Figure 7)		TBD TBD		ns ns

 Table 6.
 Switching on/off (resistive load)

Table 7. Source drain diode

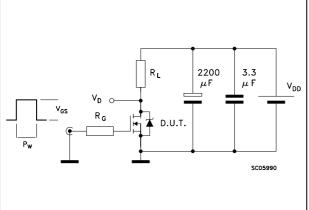
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM}	Source-drain current Source-drain current (pulsed) ⁽¹⁾				40 160	A A
V_{SD}	Forward on voltage	I _{SD} = 20 A, V _{GS} =0			1.1	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 40 A, di/dt =100 A/μs, V _{DD} = 20 V, Tj = 25 °C (<i>Figure 4</i>)		TBD TBD TBD		ns nC A

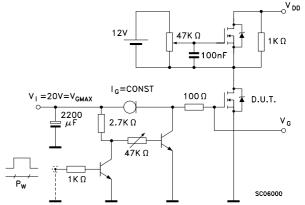
1. Pulsed: pulse duration = $300\mu s$, duty cycle 1.5%



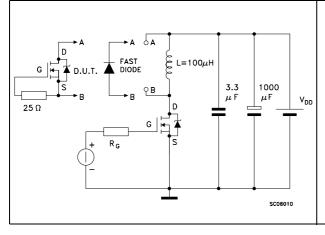
3 **Test circuits**

Figure 2. Switching times test circuit for resistive load





Test circuit for inductive load Figure 4. switching and diode recovery times



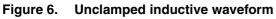
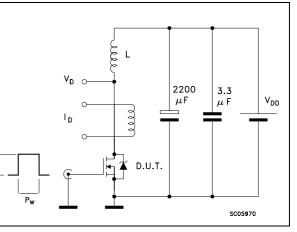


Figure 5. **Unclamped Inductive load test** circuit





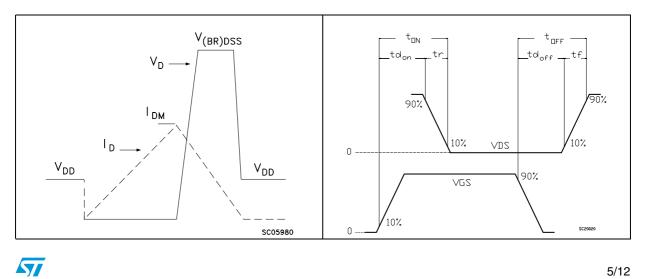
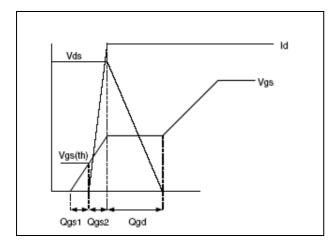


Figure 3. Gate charge test circuit

Figure 8. Gate charge waveform





4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*



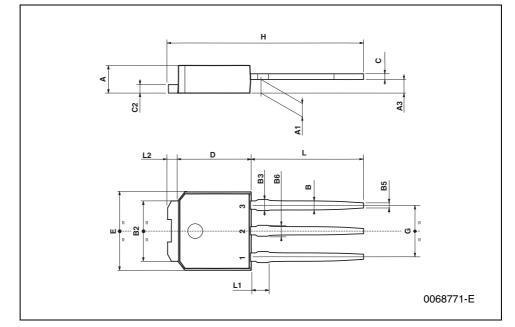
DIM		mm.			inch	
DIM.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
В	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
е		2.28			0.090	
e1	4.4		4.6	0.173		0.181
Н	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8		0.000	0.031	0.000
L4	0.6		1	0.023	0.000	0.039
R V2	0°	0.2	8°	0°	0.008	8°
		E	<u>c2</u>	- THERMAL	PAD	





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DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX
А	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
В	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
н	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047

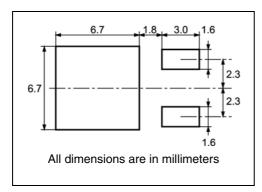




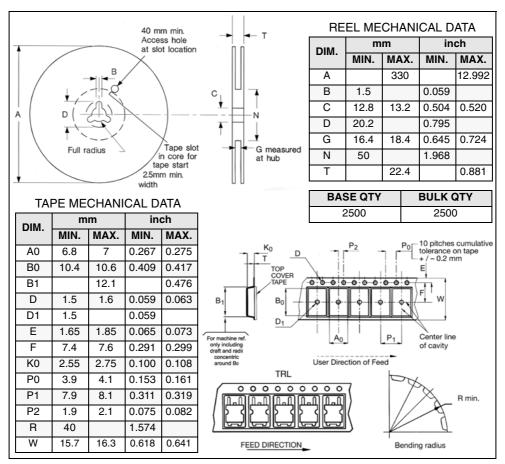
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5 Packaging mechanical data

DPAK FOOTPRINT







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6 Revision history

Table 8. Document revision history

Date	Revision	Changes	
24-Jul-2008	1	Initial release	
23-Sep-2008	2	V _{GS} value has been changed on <i>Table 2</i> and <i>Table 5</i>	



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